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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,168	12/18/2001	Ralf Dorscheid	DE000234	5133
24737	7590	11/02/2006	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			REIS, TRAVIS M	
			ART UNIT	PAPER NUMBER
			2859	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/023,168	Applicant(s) DORSCHIED ET AL.	
	Examiner Travis M. Reis	Art Unit 2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 9-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 12-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 6, 7, & 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (U.S. Patent 6292528) in view of Haruo et al. (JP 09054162 A) & Yamamoto et al. (U.S. Patent 6265782).

Wieczorek et al. disclose a detector for the detection of electromagnetic radiation, i.e. X-rays (col. 3 line 10), of which said detector includes a scintillator (11), a CMOS chip (9), and a base element (15), wherein a respective intermediate layer (13) that is defined in respect of its gap width is arranged each time between the scintillator and the CMOS chip and a layer (16) between the CMOS chip and the basic element, wherein said intermediate layers contains an adhesive (13, 16), wherein said adhesive has some quantities applied to the surface of the scintillator that faces the CMOS chip as well as to bumps that are present on the CMOS chip while said adhesive also has some quantities (16) applied directly to the rear surfaces of the CMOS chip and the basic element.

Wieczorek et al. do not disclose spacers between the scintillator and the CMOS chip.

Haruo et al. discloses an X-ray detector which discloses a photodiode array (2) and a scintillator array (3), wherein the thickness between the two arrays is regulated by spacers (5) (Figure 1) sufficient to absorb warping and roughness and to make the space uniform and improve uniformity of a detection sensitivity (ABSTRACT). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the

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spacers disclosed by Haruo et al. to the layer between the scintillator and the CMOS chip disclosed by Wieczorek et al. in order to regulate the thickness between the layers, absorb warping and roughness, and to make the space uniform and improve uniformity of a detection sensitivity.

Wieczorek et al. do not disclose spacers between the basic element and the CMOS chip.

Haruo et al. discloses the X-ray detector uses spacers between elements to regulate the roughness and warping to uniformity of the space between the elements. Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the spacers disclosed by Haruo et al. to the layer between the basic element and the CMOS chip in order that the CMOS chip be uniform when receiving the X-ray quanta (Figure 3- Wieczorek et al.)

Wieczorek does not disclose a second acrylate adhesive.

Yamamoto et al. discloses a semiconductor device, semiconductor chip mounting substrate, and method of manufacturing the device and substrate, using an adhesive comprised of the epoxy-group-containing acrylic copolymer adhesive and an additional epoxy resin used together in order to reduce the number of cracks and since it has an excellent reactivity with the epoxy resin and improves the adhesive film strength (col. 14 lines 46-64). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the epoxy-group-containing acrylic copolymer adhesive disclosed by Yamamoto et al. to the adhesive disclosed by Wieczorek in order to reduce the number of cracks and since it improves the adhesive film strength.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al., Haruo et al., & Yamamoto et al. as applied to claims 1-4, 6, 7, & 12-16 above, and further in view of Doyle et al. (U.S. Patent 6063688).

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Wieczorek et al., Haruo et al., & Yamamoto et al. disclose all of the instant claimed invention as stated above in the rejection of claims 1-4,6, 7, & 12-16, but do not disclose the spacer is a wire.

Doyle et al. discloses the fabrication of deer submicron structures and quantum wire transistors using hard-mark transistor width definition, wherein quantum wires are used as spacers for the formation of gaps/trenches in the substrate surface (col. 7 lines 50 & 55-57). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to replace the spacers disclosed by Wieczorek et al., Haruo et al., & Yamamoto et al. with spacers/wires, as taught by Doyle et al. since the spacers claimed by Applicant and the spacers used by Wieczorek et al., Haruo et al., & Yamamoto et al. are alternate types of spacers which will perform the same function, if one is replaced with the other, of creating gaps between dielectric elements.

Wieczorek et al., Haruo et al., Yamamoto et al., & Doyle et al. do not disclose the spacer/wire consists of the materials Au and AlSi. However, the particular type of material used to make the spacers/wires, absent any criticality, is only considered to be the use of a “preferred” or “optimum” material out of a plurality of well known commonly available, low-cost materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on the intended use of Applicant's apparatus, i.e., suitability for the intended use of Applicant's apparatus, and since the courts have stated that a selection of a material on the basis of suitability for intended use of an apparatus would be entirely obvious. See In re Leshin, 125 USPQ 416 (CCPA 1960). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to make the spacers disclosed by Wieczorek et al., Haruo et al., Yamamoto et al., & Doyle et al. out of Au and AlSi in order to reduce

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manufacturing costs.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al., Haruo et al., & Yamamoto et al. as applied to claims 1-4,6, 7, & 12-16 above, and further in view of Boedinger et al. (U.S. Patent 6149478).

Wieczorek et al., Haruo et al., & Yamamoto et al. disclose all of the instant claimed invention as stated above in the rejection of claims 1-4,6, 7, & 12-16, but do not disclose the basic element is a ceramic element based on aluminum oxide.

Boedinger et al. disclose a method of manufacturing large crystal bodies, (i.e. scintillators) using aluminum oxide for the reflection layer of the lining/base element (col. 2 lines 41-45). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to make the basic element disclosed by Wieczorek et al. out of aluminum oxide in order to provide a suitable reflection surface for the scintillator.

Response to Arguments

5. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to add spacers taught by Haruo et al. to the layers disclosed by Wieczorek to provide uniformity when receiving X-ray quanta is sufficient motivation for the modification.

6. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., complete

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expulsion of air bubbles) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Hence, there is no need for Haruo et al. to teach such an expulsion of air bubbles.

7. In response to applicant's arguments that Wieczorek must be interpreted as implying a teaching of manufacturing a uniform and air-free adhesive layer in view of the failure of Wieczorek to teach spacers; these arguments have been fully considered but they are not persuasive since Wieczorek does not disclose knowledge of Haruo and thus such an implication is purely speculative, furthermore the combination of Wieczorek & Haruo is based on the motivation of regulated thickness and nothing to do with a motivation of "air free adhesive layers".

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Travis M. Reis whose telephone number is (571) 272-2249. The examiner can normally be reached on 8--5 M--F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

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would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Travis M Reis
Examiner
Art Unit 2859

Diego Gutierrez
Supervisory Patent Examiner
Tech Center 2800

tmr
October 26, 2006